Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1 (currently amended): A power supply clamp circuit for preventing damage to integrated circuits when electrostatic discharge occurs at a first voltage source of the integrated circuits, the integrated circuits further comprising a second voltage source that is independent from the first voltage source and having the same voltage as the first voltage source, the power supply clamp circuit comprising:

a first voltage generator electrically connected to a first node for generating a voltage;

a first PMOS transistor having a source electrically connected to the first voltage source, a gate electrically connected to the first node, and a drain electrically connected to a second node;

a first NMOS transistor having a drain electrically connected to the second node, a gate electrically connected to the first node, and a source connected to ground;

a second NMOS transistor having a drain electrically connected to the first voltage source, a gate electrically connected to the second node, and a source connected to ground; and

a second PMOS transistor having a source electrically connected to the second node, a gate and a drain both electrically connected to the first node.

2 (original): The power supply clamp circuit of claim 1 wherein a drain of the second NMOS transistor of the power supply clamp circuit has P+ implantation dosage in an ion implantation process.

3 (original): The power supply clamp circuit of claim 1 wherein the first voltage generator of the power supply clamp circuit comprises:

a resistor having one end of the resistor electrically connected to the first voltage source and another end of the resistor electrically connected to the first node; and

a capacitor having one end of the capacitor electrically connected to the first node and another end of the capacitor connected to ground.

4 (original): The power supply clamp circuit of claim 3 wherein the resistor of the first voltage generator comprises metal wiring.

5 (original): The power supply clamp circuit of claim 3 wherein the capacitor of the first voltage generator comprises an NMOS transistor having a drain and a gate electrically connected to a substrate.

6-8 (cancelled).

9 (previously presented): A power supply clamp circuit for preventing damage to integrated circuits when electrostatic discharge occurs at a first voltage source of the integrated circuits, the power supply clamp circuit comprising:

a first PMOS transistor having a source electrically connected to the first voltage source, a gate electrically connected to a first node, and a drain electrically connected to a second node;

a first NMOS transistor having a drain electrically connected to the second node, a gate electrically connected to the first node, and a source connected to ground;

a second NMOS transistor having a drain electrically connected to the first voltage source, a gate electrically connected to the second node, and a source connected to ground;

a second voltage source being independent from a first voltage source and having the same voltage as the first voltage source;

a resistor with one end of the resistor electrically connected to the second voltage source and another end of the resistor electrically connected to a third node;

a second PMOS transistor having a source electrically connected to the third node, a gate electrically connected to a fourth node, and a drain electrically connected to the first node; and

a third NMOS transistor having a drain and a gate commonly electrically connected to the fourth node, and a source connected to ground.

10 (previously presented): The power supply clamp circuit of claim 9 wherein the drain of the second NMOS transistor of the power supply clamp circuit has P+ implantation dosage in an ion implantation process.

11 (previously presented): The power supply clamp circuit of claim 9 wherein the resistor of the power supply clamp circuit comprises metal wiring.

12 (cancelled).

13 (new): The power supply clamp circuit of claim 1 wherein, the second voltage source comprises:

a resistor with one end of the resistor electrically connected to the second voltage source and another end of the resistor electrically connected to a third node;

a third PMOS transistor having a source electrically connected to the third node, a gate electrically connected to a fourth node, and a drain electrically connected to the first node; and

a third NMOS transistor having a drain and a gate commonly electrically connected to the fourth node, and a source connected to ground.

14 (new): The power supply clamp circuit of claim 13 wherein a drain of the second

NMOS transistor of the power supply clamp circuit has P+ implantation dosage in an ion implantation process.

15 (new): The power supply clamp circuit of claim 13 wherein the resistor of the second voltage source comprises metal wiring.